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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/738,347	12/17/2003	Bertrand Gabillard	FR920020081US1	9674

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EXAMINER	
NGUYEN, JOHN B	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 12/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/738,347	GABILLARD ET AL.	
	Examiner	Art Unit	
	John B Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12/17/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Koch U.S Patent Number 5,057,839.

2. Regarding to claims 1-10, Figure 1, Koch discloses a circuit comprising: a differential sampling circuit (fig. 1) employing a switched-capacitor approach for generating a real differential input signal DC offset value at each period of a system clock, the circuit having first and second input signals (E, E') input thereto, the circuit comprising: a differential operational amplifier (OP1) having a positive input (E') and a negative input (E), the positive output generating a first output signal (+) and the negative output generating a second output signal (-) defining a differential output signal AVout therebetween;

a first switched-capacitor network including: a first capacitor (C12') coupled to the positive input and to a first node, a first switch (S8') coupled to the first node and to a first terminal supplying the first input signal (E'), a second switch (S6') coupled to the first node and to ground, a third switch (S1') coupled to the positive input and to the negative output, a fourth switch (S22') coupled to the negative output and to a second node, a fifth switch (S23') coupled to the second

node and to ground; a second capacitor (C1') coupled to the positive input and to the second node, a sixth switch (S2') coupled to the first node and to the negative output, a third capacitor (C11') coupled to the positive input and to a third node, a seventh switch (S5') coupled to the third node and to ground, and an eighth switch (S7') coupled to the first node and to the third node;

a second switched-capacitor network including: a fourth capacitor (C12) coupled to the negative input and to a fourth node, a ninth switch (S8) coupled to the fourth node and to a second terminal supplying the second input signal (E), a tenth switch (S6) coupled to the fourth node and to ground, an eleventh switch (S1) coupled to the negative input and to the positive output, a twelfth switch (S22) coupled to the positive output and to a fifth node, a thirteenth switch (S23) coupled to the fifth node and to ground, a fifth capacitor (C1) coupled to the negative input and to the fifth node, a fourteenth switch (S2) coupled to the fourth node and to the positive output, a sixth capacitor (C11) coupled to the third negative input and to a sixth node, a fifteenth switch (S5) coupled to the sixth node and to ground, and a sixteenth switch (S7) coupled to the fourth node and to the sixth node;

wherein

the first capacitor and the third capacitor have equal values, the fourth capacitor and the sixth capacitor have equal values, and the switches are selectively set in response to control signals in either an open or a closed state according to a determined algorithm within one period of the system clock (fig.1, columns 3-5) .

3. Regarding to claim 2, wherein the control signals are generated by timing control means receiving the system clock (fig.1, columns 3-5).

4. Regarding to claim 3, wherein the first, ninth, third, eleventh, fifth, and thirteenth switches are closed while the second, tenth, fourth, twelfth, sixth, fourteenth, seventh, fifteenth, eighth and sixteenth switches are open during at least a first portion of the first half period (fig.1, columns 3-5).

5. Regarding to claim 4, wherein the second, tenth, fourth, and twelfth switches are closed while the first, ninth, third, eleventh, fifth, thirteenth, sixth, fourteenth, seventh, fifteenth, eighth and sixteenth switches are open during at least a second portion of the first half period (fig.1, columns 3-5).

6. Regarding to claim 5, wherein the first, ninth, third, eleventh, seventh, and fifteenth switches are closed while the second, tenth, fourth, twelfth, fifth, thirteenth, sixth, fourteenth, eighth and sixteenth switches are open during at least a first portion of the second half period (fig.1, columns 3-5).

7. Regarding to claim 6, wherein the fifth, thirteenth, sixth, fourteenth, eighth, and sixteenth switches are closed while the first, ninth, second, tenth, third, eleventh, fourth, twelfth, seventh and fifteenth switches are open during at least a second portion of the second half period (fig.1, columns 3-5).

8. Regarding to claim 7, Figure 1, Koch discloses a circuit comprising: a differential operational amplifier (OP1) having an input terminal (E) and an output terminal (+), and characterized by a DC offset voltage; a first capacitor (C12) and a second capacitor (C11) each having a first terminal and a second terminal, each of the first terminal being connected to the input terminal, the first capacitor and the second capacitor being matched with respect to capacitance value; wherein the charge on the first capacitor (C12) is proportional to the DC offset voltage

during an input signal sampling operation in a portion of each system clock period, and the first capacitor and the second capacitor are connected in parallel during a charge transfer operation in a subsequent portion of each system clock period (fig.1, column 3-5).

9. Regarding to claim 8, wherein an output terminal voltage during the charge transfer operation is proportional to a sum of a first input voltage applied to the input terminal during a first signal sampling operation and a second input voltage applied to the input terminal during a second signal sampling operation in another portion of the system clock period, the output terminal voltage being independent of the DC offset voltage (fig. 1, column 3-5).

10. Regarding to claim 9, wherein each period of the system clock comprises a first half period and a second half period, the first input signal sampling operation is during the first half period, the second input signal sampling operation is during the second half period, and the charge transfer operation is subsequent to the second input signal sampling operation during the second half period (fig. 1, column 3-5).

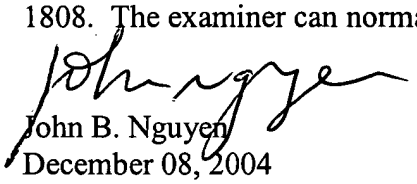
11. Regarding to claim 10, further comprising a plurality of switches so that the first capacitor, the second capacitor and the switches form a switched-capacitor network, and wherein the switches are selectively set in response to control signals in either an open or a closed state according to a determined algorithm within one period of the system clock (fig. 1, column 3-5).

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. (See enclosed Form PTO-892).

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to John B Nguyen whose telephone number (571) 272-1808. The examiner can normally be reached on 8AM-4: 30 PM M-F.



John B. Nguyen
December 08, 2004